

REMARKS/ARGUMENTS

The Applicant originally submitted Claims 1-20 in the application. In a previous response, the Applicant amended independent Claims 1, 8, and 15 to include the limitations from dependent Claims 5, 12, and 19 and canceled without prejudice or disclaimer dependent Claims 5, 12, and 19. In the present response, no claims have been amended, canceled, or added. Accordingly, Claims 1-4, 6-11, 13-18, and 20 are currently pending in the application.

I. Formal Matters and Objections.

The Examiner has objection to Claims 1 and 15 for lack of antecedent basis. The Applicant is perplexed and does not know how to respond in light of the following from MPEP §2173.05(h)(I.):

Alternative expressions are permitted if they present no uncertainty or ambiguity with respect to the question of scope or clarity of the claims. One acceptable form of alternative expression, which is commonly referred to as a Markush group, recites members as being "selected from the group consisting of A, B, and C." See *Ex parte Markush*, 1925 C.D. 126 (Comm'r Pat. 1925).

II. Rejection of Claims 1-4, 8-11 and 15-18 under 35 U.S.C. §103

The Examiner has rejected Claims 1-4, 8-11 and 15-18 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,689,516 to Mack, *et al.* ("Mack") in view of U.S. Patent No. 5,515,523 to Kalkunte, *et al.* ("Kalkunte"). The Applicant respectfully disagrees.

The Examiner asserts that Mack teaches a system for securing the integrated circuit (IC) against subsequent reprogramming including port inhibit circuitry modifiable to achieve a configuration that determines an extent to which a testing port is enabled, wherein the extent selected from the group consisting of fully disabled and completely disabled. The Examiner recognizes that

Mack is silent on partially disabling a testing port and cites Kalkunte to cure this deficiency. (*See* Examiner's Action of January 10, 2008, page 3.) Mack teaches a programmable logic device (PLD) includes test circuitry compatible with the JTAG standard which includes a programmable JTAG-disable bit that can be selectively programmed to disable the JTAG circuitry, leaving the PLD to operate as a conventional non-JTAG-compatible PLD. (*See*, for example, Abstract.) Thus, Mack teaches a system for securing an IC against subsequent reprogramming a PLD array which includes JTAG test circuitry by programming a JTAG-disable bit which disables the JTAG test circuitry but continues to allow normal access to the PLD by a user.

Kalkunte, as applied by the Examiner, teaches a memory controller 20 monitors memory transfers requested by bus A interface 30. If a volume of requests indicates that FIFOs contained in bus A interface 30 may be significantly backed up, then memory controller 20 partially disables the memory transfers with bus B interface 40. When bus B interface 40 is partially disabled, a predetermined number of requests from bus A interface 30 will be granted before one request (if pending) from bus B interface 40 will be granted. (*See*, for example, column 6, lines 4-13 and Figure 2.) Thus, Kalkunte teaches that while bus B interface 40 is partially disabled, bus A interface 30 can still be used to access a memory array.

The Examiner states that it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teaching of Mack as taught by Kalkunte in order to "maximize efficient use of the memory component and minimized starvation of other memory ports, without requiring higher performance memory components or wider memory bus widths." (*See* Examiner's Action of January 10, 2008, page 3.) The invention as presently claimed, however, is not concerned with maximizing efficient use of a memory component but, rather, eliminating access to a

memory or other component. Additionally, the Applicant fails to find where Kalkunte is concerned with the extent to which a testing port is partially disabled, but, rather a memory port.

Furthermore, modifying Mack with Kalkunte would render Mack unsatisfactory for its intended use. Since Kalkunte allows access to a memory array by one memory bus when another memory bus is partially disabled, a user could still program the memory array. If a user can access the memory of Mack even when partially disabled as taught by Kalkunte, the JTAG disable bit could be changed, re-enabling the JTAG circuitry. MPEP §2143.01 states that "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).

As such, for at least these reasons, the cited combination of Mack and Kalkunte, as applied by the Examiner, does not establish a *prima facie* case of obviousness of independent Claims 1, 8, and 15 and Claims that depend thereon. Accordingly, the Applicants respectfully request the Examiner to withdraw the §103(a) rejection of Claims 1-4, 8-11 and 15-18 and allow issuance thereof.

III. Rejection of Claims 6 and 13 under 35 U.S.C. §103

The Examiner has rejected Claims 6 and 13 under 35 U.S.C. §103(a) as being unpatentable over Mack in view of Kalkunte and further in view of the U.S. Patent No. 7,124,340 to Bos, *et al.* ("Bos") The Applicant respectfully disagrees.

As established above, the cited combination of Mack and Kalkunte does not provide a *prima facie* case of obviousness of independent Claims 1 and 8. Bos has not been cited to cure the

deficiency of the cited combination but to teach wherein the testing port comprises a direct loopback between input and output pins thereof. (See Examiner's Action of January 10, 2008, page 5.) Additionally, the Applicant does not find where Bos cures the above-noted deficiencies of the cited combination of Mack and Kalkunte. As such, the cited combination of Mack, Kalkunte, and Bos does not establish a *prima facie* case of obviousness of now amended independent Claims 1 and 8 and Claims that depend thereon. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §103(a) rejection of Claims 6 and 13 and allow issuance thereof.

IV. Rejection of Claims 7, 14, and 20 under 35 U.S.C. §103

The Examiner has rejected Claims 7, 14, and 20 under 35 U.S.C. §103(a) as being unpatentable over Mack in view of Kalkunte and further in view of U.S. Patent No. 6,522,100 to Hansford ("Hansford"). The Applicant respectfully disagrees.

As established above, the cited combination of Mack and Kalkunte does not provide a *prima facie* case of obviousness of independent Claims 1, 8, and 15. Hansford has not been cited to cure the above-noted deficiencies of the cited combination of Mack and Kalkunte but to teach wherein the IC is a baseband chip of a mobile communications device. (See Examiner's Action of January 10, 2008, page 5.) Additionally, the Applicant does not find where Hansford cures the above-noted deficiencies of the cited combination of Mack and Kalkunte. As such, the cited combination of Mack, Kalkunte, and Hansford does not establish a *prima facie* case of obviousness of now amended independent Claims 1, 8, and 15 and Claims that depend thereon. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §103(a) rejection of Claims 7, 14, and 20 and allow issuance thereof.

V. Conclusion

In view of the foregoing remarks, the Applicant now sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-4, 6-11, 13-18, and 20.

The Applicant requests the Examiner to telephone the undersigned agent of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

HITT GAINES, PC

A handwritten signature in black ink that reads "Steven J. Hanke". The signature is written in a cursive, flowing style.

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